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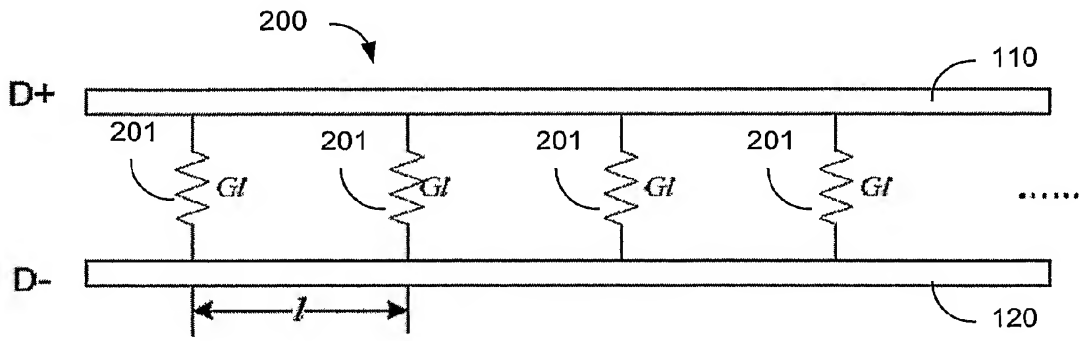
(54) Title: ELECTRICAL SIGNALING VIA DIFFERENTIAL TRANSMISSION LINE



(57) Abstract: Designs and techniques for transmitting electrical signals via transmission lines on integrated circuits without distortion and at the speed of light. In one implementation, one or more leakage resistors (201) are connected between the two conductor wires of a transmission line.

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ELECTRICAL SIGNALING VIA DIFFERENTIAL TRANSMISSION LINE

Background

[0001] This application relates to differential transmission lines in circuits such as integrated circuits.

[0002] Electronic circuits use electrically conducting paths or interconnects to interconnect various circuit elements. The properties of such interconnects, especially the global interconnects, are known to have significant or even dominating impact on the circuit performance and the power consumption. Therefore, the designs and engineering of the interconnects have attracted much attention in the field of electronics, especially in integrated circuits.

[0003] In many integrated circuits, various interconnects are implemented by inverter repeated RC wires. In this design, each interconnect is basically multiple conductive wires that are interconnected by inverters. The RC responses of such interconnects cause latency in the electrical signaling and the latency increases as integrated circuits operate at increasingly higher clock frequencies. In some applications, the inverter repeated RC wires can no longer keep up with the pace of advances in transistor speed at a satisfactory cost of power consumption. See, e.g., R. Ho, K. W. Mai, and M. A. Horowitz, "The Future of Wires," Proc. of IEEE, vol. 89, No. 4, pp. 490-504 (2001).

[0004] Several interconnects for integrated circuits have been developed as alternatives to the inverter repeated RC wires, including on-chip optical interconnects and RF wireless interconnects. See, e.g., N. M. Jokerst et al., "The Heterogeneous Integration of Optical Interconnections Into Integrated Microsystems," IEEE Journal of Selected Topics in Quantum Electronics, Vol. 9, No. 2, pp. 350-360 (2003) and M. F. Chang, V. P. Roychowdhury, L. Zhang, H. Shin, and Y. Qian, "RF/Wireless Interconnect for Inter- and Intra-Chip

Communications," Proceedings of the IEEE, vol. 89, no. 4, pp. 456-466 (2001).

Summary

[0005] This application describes, among others, distortionless differential transmission lines for transmitting signals at the speed of light. In one implementation, a device is described to include a first conductor and a second conductor to form a differential transmission line to transmit an electrical signal; and leakage resistors connected between the first and second conductors at different positions along the differential transmission line to make a phase velocity and a signal attenuation of the electrical signal to be independent of a frequency of the electrical signal.

[0006] In another implementation, a device includes a first conductor and a second conductor to form a differential transmission line to transmit an electrical signal; and leakage resistors connected between the first and second conductors at different positions along the differential transmission line. Each leakage resistor has a conductance per one unit length of RC/L, where R, C and L are effective resistance, capacitance and inductance of the differential transmission line per one unit length, respectively.

[0007] In yet another implementation, a method includes using at least two conductors to form a differential transmission line to guide a signal; and connecting a plurality of leakage resistors at different locations along the differential transmission line to connect the two conductors to make the phase velocity and attenuation of the signal in the transmission line independent of a frequency of the signal.

[0008] These and other implementations and their applications are described in greater detail in the attached drawings, the following detailed description, and the claims.

Brief Description of Drawings

[0009] FIGS. 1A and 1B show an example of a lossy differential transmission line.

[0010] FIGS. 2A, 2B and 2C show an example of a distortionless differential transmission line having leakage resistors connected along the transmission line to provide leakage conductance between the two conductors that form the transmission line.

[0011] FIGS. 3 and 4 show simulated transmission properties of the transmission lines with and without the leakage resistors.

[0012] FIG. 5 shows simulated tolerance properties of the transmission lines with the leakage resistors in presence of variations from the optimized values, where the horizontal axis is in a percentage of a change in G from the optimized value.

[0013] FIG. 6 shows two exemplars for the leakage resistors in FIGS. 2A.

[0014] FIGS. 7A, 7B, 7C, 8A, 8b and 9 show examples of conductor arrangements for distortionless differential transmission lines with leakage resistors.

[0015] FIGS. 10 and 11 show eye diagrams of the distortionless differential transmission line in FIG. 9 with two different numbers of leakage resistors.

[0016] FIG. 12 shows one example of a clock distribution circuit using distortionless differential transmission lines with leakage resistors.

Detailed Description

[0017] Electrical signaling over on-chip transmission lines is one of the most attractive solutions for high performance on-chip communications. See, e.g., B. M. Beckmann, and D. A. Wood, "TLC: Transmission Line Caches," 36th IEEE International Symposium on Microarchitecture (2003). Comparing with traditional inverter repeated RC wires, the transmission line has a number of advantages. For example, the signal propagates at the speed of light on a transmission line. The transmission line can be used to achieve higher throughput at lower latency. For another example, the transmission line signaling has much smaller power consumption than the repeated RC wires because the forced swing of wire capacitance in the repeated RC wires is eliminated in the transmission line.

[0018] One challenge to the implementation of transmission line for on-chip communication is the resistive nature of the impedance of on-chip metal wires. The high resistance causes significant frequency dependency on both the wave propagation speed and attenuation. For random binary bits input, the spectrum of input waveform spans over a large spectral range. Within this spectral range, the phase velocity and attenuation of the signals varies significantly as the frequency changes. See, e.g., R. T. Chang, N. Talwalkar, C. P. Yue, and S. S. Wong, "Near Speed-of-Light Signaling Over On-Chip Electrical Interconnects", IEEE Journal of Solid-State Circuits, vol. 38, No. 5, pp. 834-838 (2003). This feature causes the wave form to exhibit excessive dispersion through the process of wave propagation. One of the consequences of this dispersion is the inter symbol interferences (ISI) which in turn lead to significant data dependant jitters and limit the throughput of the communications.

[0019] The differential transmission lines of this application may be used to provide on-chip electrical signaling in various integrated circuits to preserve the original wave form of a

signal and to transmit the signal at the speed of light, independent of its frequency. Specific examples are described below for implementations of a differential transmission line with spatially distributed leakage conductance along the transmission line via leakage resistors connected between two conductor wires of each differential pair in the transmission line. The leakage resistors between the wires of a differential pair are intentionally inserted into the transmission line. The resistance value of each leakage resistor is set to achieve a transmission speed for all frequency components of a signal at the speed of light in the dielectric material surrounding the transmission line and to achieve a "distortionless" transmission by minimizing the signal dispersion, i.e., distortions between different signal components at different signal frequencies in the signal.

[0020] FIG. 1A shows an example of a differential transmission line 100 having a pair of conductors or conductor wires 110 and 120 to connect a signal driver 101 at one end and a signal receiver 102 at the other end. The two conductors 110 and 120 are separated and electrically insulated from each other everywhere except at the driver 101 and the receiver 102. The signal driver 101 has two terminals that are respectively connected to the two conductors 110 and 120. A signal from the signal driver 101 is applied in form of two differential voltages on the two conductors 110 and 120, respectively. The signal propagates through the two conductors 110 and 120 to reach the receiver 102.

[0021] The differential transmission line 100 has resistance and inductance in each conductor. In actual circuits, shunt capacitance exists between two conductors 110 and 120. These parameters of the transmission line 100 can be represented by R, C and L as the effective resistance, capacitance and inductance of the differential transmission line per one unit length, respectively. Accordingly, there is

loss of the electrical current through the shut capacitance between the two conductors 110 and 120. FIG. 1B shows an equivalent circuit of the transmission line with two conductors 110 and 120 in FIG. 1 to show the resistance, the inductance and the shunt capacitance. Such a transmission line exhibits dispersion and the phase velocity of the signal and the attenuation of the signal both vary with the signal frequency. Hence, different signal components at different frequencies have different phase velocities and experience different attenuations when propagating along the transmission line. An electronic pulse has multiple spectral components at different frequencies and as such will be distorted after propagation through this transmission line 100. Therefore, the signal is distorted at the receiver 102.

[0022] FIGS. 2A, 2B and 2C illustrate one example of the distortionless transmission line 200 with intentionally inserted leakage resistors 201 between the two conductors 110 and 120 along the transmission line to eliminate or minimize the dispersion and thus the signal distortion. FIG. 2A shows the structure of a portion of the transmission line 200. In this particular example, the two conductors 110 and 120 are parallel to each other. In many implementations on chips, the two conductors 110 and 120 are parallel to the substrate. Each leakage resistor 201 is connected between the two connectors 110 and 120. Multiple leakage resistors 201 are connected along the transmission line 200. In the specific examples described here, the leakage resistors 201 may be equal in resistance and evenly spaced along the transmission line with a spacing l between two adjacent leakage resistors 201.

[0023] FIG. 2B shows an equivalent circuit of the transmission line 200 to illustrate the resistance, the inductance, the shunt capacitance and the inserted leakage resistance. FIG. 2C shows an equivalent discrete RLGC circuit model for

is represented by the corresponding leakage conductance G per one unit length. It is assumed that R, L, G, C are frequency-dependant constants. The jitter caused by the frequency dependency of R, L, G, C is not significant for on-chip interconnect applications.

[0024] The signal wave in the transmission line 200 is described as the function of distance z along the transmission line, and time t, by the Telegrapher's equations:

$$\frac{dV(z,t)}{dz} = -RI(z,t) - L\frac{dI(z,t)}{dt} \qquad (1)$$

$$\frac{dI(z,t)}{dz} = -C\frac{dV(z,t)}{dt} \qquad (2)$$

For a sinusoidal signal of angular frequency ω, the propagation of the incident wave along the transmission line 200 can be expressed as:

$$V(z,t) = V_0 e^{-\alpha z - j\beta z + j\omega t} \qquad (3)$$

where α and β are respectively the real and imaginary parts of the propagation function γ which is defined as:

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} = \alpha + j\beta, \qquad (4)$$

Equation (3) shows that the exponential, $e^{-\alpha}$, of the real part of the propagation function represents the unit distance attenuation of the transmission line. The imaginary part β of the propagation function γ corresponds to the phase shift of the wave along the transmission line 200. The phase velocity of the incident wave is $\upsilon = \omega/\beta$.

from Equation (4):

$$\alpha = \sqrt{\frac{1}{2}}\sqrt{RG - \omega^2 LC + \sqrt{(RG - \omega^2 LC)^2 + \omega^2 (LG + RC)^2}} \quad (5)$$

$$\beta = \sqrt{\frac{1}{2}}\sqrt{\omega^2 LC - RG + \sqrt{(RG - \omega^2 LC)^2 + \omega^2 (LG + RC)^2}} \quad (6)$$

Equations (5) and (6) show that, when there is no leakage conductance (G = 0), which is the common practice in the on-chip transmission line because silicon dioxide is a very good insulator, the attenuation (α) and phase velocity ($\upsilon=\omega/\beta$) depend on the frequency ω, especially when the wire resistance, R, is comparable to or larger than the impedance contributed by wire inductance, ωL.

[0026] Notably, when the leakage conductance of each leakage resistor is set at G = RC/L, the attenuation and the phase velocity are independent of the signal frequency based on Equations (5) and (6). Under this condition, different signal spectral components travel at the same speed (the speed of light) and experience the same attenuation when propagating in the transmission line 200. The signal, therefore, is not distorted. In this context, the transmission line 200 provides a distortionless transmission.

[0027] Under the condition of G = RC/L, the parameters α and β can be expressed as follows:

$$\alpha = R/\sqrt{L/C} \quad (7)$$

$$\beta = \omega\sqrt{LC} \quad (8)$$

velocity υ, and the attenuation of the transmission line 200 can be respectively written in the following equations:

$$Z_0 = \sqrt{\frac{L}{C}} \qquad (9)$$

$$v = \frac{1}{\sqrt{LC}} = c \qquad (10)$$

$$A(z) = e^{-\frac{R}{Z_0}z} \qquad (11)$$

The distortionless transmission line has pure resistive characteristic impedance as in Equation (8). The phase velocity is exactly the speed of light in the dielectrics as expressed in Equation (10). According to Equation (11), the attenuation depends on the ratio between wire resistance R and characteristic impedance Z_0. For typical on-chip transmission line implemented on the upper low impedance metal layers, the resistance of a wire with a width of several microns can be less than 10 ohm/mm, and the characteristic impedance of transmission line may be around 100 ohm. Thus, an input signal with magnitude of 1.0V may have a magnitude of 135 mV after traveling a distance of 2 cm. A sense amplifier may be used to detect the output signal at this magnitude. A. Maheshwari and W. Burleson described examples of sense amplifiers in their article "Differential Current-Sensing for On Chip Interconnects," IEEE Transactions on VLSI, Vol. 12, No. 12, pp. 1321-1329 (2004).

[0028] In various implementations, e.g., on-chip wires, the leakage resistors or conductors can be inserted between two wires or conductors of a differential pair to realize the constant leakage conductance G of RC/L per unit length for the transmission line. In some implementations, equal valued

resistors can be connected between the two conductors and spaced evenly from one another along the transmission line. The spacing l between two adjacent leakage resistors can be a constant for all leakage resistors 201, i.e., a leakage conductor with conductance Gl is periodically insert at every distance l in the z direction along the transmission line. When the interval l is small enough comparing with the wavelength of the data signal, the discontinuity caused by this discrete resistor insertion scheme is ignorable. Simulation results suggest that, when l is equal to or less than $ct_p/20$, the jitter caused by ISI is smaller than 5% of the clock period, where t_p is a clock period of the signal and c is a speed of light in a dielectric material surrounding the transmission line. In general, the jitter decreases with the interval l. When the interval l increases, the jitter increases. The actual interval l between two adjacent leakage resistors for a specific implementation of the differential transmission line 200 in FIG. 2A can be selected according to the acceptable jitter for the implementation.

[0029] Other configurations for implementing the constant leakage conductance G of RC/L per unit length for the transmission line are also possible. For example, different leakage resistors placed along the transmission line may have different conductance or resistance values from one another as long as the effective leakage conductance per unit length is RC/L. As another example, the leakage resistors may not be evenly spaced along the transmission line and the spacings may vary. The constraint is that the product of the interval length and the leakage resistance is a constant given by L/RC.

[0030] FIG. 3 illustrates the characteristics of a differential pair of 2cm-length and 4-μm width wires. Significant changes in the attenuation and phase velocity are present. When the leakage or shunt conductance is zero (G = 0), the attenuation ranges from 0.9997 at 1 KHz to 0.644 at 1

GHz. The speed or phase velocity ranges from 9.0×10^7 mm/s at 1KHz to 8.5×10^{10} mm/s at 1 GHz. The curve saturates at the speed of light 1.8×10^{11} mm/s when the frequency is about 1T Hz. For the proposed distortionless pairs, the attenuation is 0.4147 and the phase velocity is at the speed of light. These two curves are flat.

[0031] FIG. 4 shows the dispersion effects on a square pulse wave that propagates through a differential transmission line without the leakage resistors shown in FIG. 2 (G-0) and a similar differential transmission line with the leakage resistors shown in FIG. 2 (G=RC/L). The input is the square wave at left, which rises at 50ps. When shunt conductance G = 0, the output disperses on the rising and falling edges. A long tail appears at the falling edge of the pulse due to the dispersion and is the main cause of the intersymbol interference. Because the digital signals include signal components at different frequencies, the distortion causes interferences among adjacent symbols. The intersymbol interference is one limiting factor of the performance of the transmission lines.

[0032] When the leakage resistors are present and set at G= RC/L, the transmission line behaves differently. As illustrated in FIG. 4, the pulse wave form is preserved after the propagation. The magnitude of the signal, however, drops. The rising edge starts at 161 ps the same rising time as the wires with no shunts. However, the output pulse substantially maintains the original square waveform without significant distortions. The delay is 161- 50 = 111 ps, and is the time for the signal to travel at the speed of light, which is about 1.8×10^{11} mm/s for a length of 2 cm along the transmission line.

[0033] The performance of the distortionless transmission line 200 is relatively insensitive to deviations of the values of the leakage resistors 201 from the optimized value of G =

RC/L. For example, the leakage resistors 201 may not have the same resistance and the value of each leakage resistor may be different from the ideal conductance value of G=RC/L. Various factors may cause such deviations, such as variations in the fabrication process and variations in the voltage and the temperature at different locations of the transmission line. Assume that the leakage conductance G of a leakage resistor varies from the perfectly matched or optimized conductance value RC/L by a factor Δ, i.e. $G = (1 + \Delta)RC/L$. Under the approximation with the first order Taylor's expansion, the frequency dependency of the attenuation and phase velocity can be expressed as:

$$\alpha = \frac{R}{\sqrt{L/C}}\left(1 + \frac{1}{2}\Delta - \frac{1}{8}\frac{R^2}{R^2 + \omega^2 L^2}\Delta^2\right), \quad v = \frac{1}{\sqrt{LC}}\left(1 - \frac{1}{8}\frac{R^2}{R^2 + \omega^2 L^2}\Delta^2\right). \tag{12}$$

[0034] In Equation (12), the frequency dependent terms of the attenuation and phase velocity occur not at the first order but rather at the second order of the frequency. Hence, the attenuation and the phase velocity are relatively insensitive to variations in frequency. The attenuation constant has a first order term independent of the frequency and this first order term does not contribute to the distortion. For the phase velocity, the first order term is zero. Therefore, the shunt conductance G = RC/L is a solution to minimize the skew sensitivity. Applying a similar procedure, for the given shunt conductance G = RC/L, the serial resistance R is a solution to minimize the skew sensitivity.

[0035] The coefficients of the second order terms in Equation (12) are limited by an upper bound factor of 1/8. Suppose that the shunt conductance changes by ten percent, i.e. Δ=0.1. The third order terms in Equation (12) deviate by no more than

$\Delta^2/8 \approx 0.0012$. Therefore, the distortionless wires can distribution multi-gigahertz clock within comfortable design space. This tolerance of the transmission line 200 to variations is one of the advantages of the present design.

[0036] FIG. 5 shows variations in the phase velocity when G varies from its designed value of RC/L by up to 10% for a 3um wide on-chip wire when the frequency changes from 10 MHz to 10 GHz. Hence, when G stays at its nominal value, i.e. variation equals to 0, the changes of phase velocity and attenuation between 10 MHz and 10 GHz are all 0. When G has a 10% variation, there is less than 1% change in the speed and less than 5% variations in the signal amplitude. This tolerance of the transmission line 200 to variations is one of the advantages of the present design

[0037] A high-speed distortionless transmission line based on the design in FIG. 2A may be fabricated by various methods, including the various silicon processes. As an example, our research results suggest that the 65-nm silicon fabrication technology can be used to construct such a distortionless transmission line integrated on a silicon chip to achieve a data rate of 15 Gbits/s over a 20-mm on-chip serial link without any equalization. The jitter caused by the communication over the 20-mm transmission line is lower than 10 ps. The average power consumption of the data transportation through the 20-mm transmission line can be as low as 3.1pJ/bit. The wiring channel requires less than an area of 1000 μm^2 on poly for a 20-mm long serial link. In some implementations, the use of this distortionless transmission line may reduce the transmission delay by six times and reduce the power consumption by 85% in comparison with electrical signaling via a conventional repeated RC wire.

[0038] Implementations of the present transmission line approach may be configured to achieve one or more advantages over other on-chip signaling schemes. One advantage, for

example, is that the signal propagation on the distortionless transmission line is exactly the speed of light. This property is attractive for the connections with extreme requirement on the signal latency, such as the global control signal in a large processor or the global data communication in a large network-on-chip. Also, the waveform essentially remains undistorted at the receiver end after propagation through the transmission line and there is no inter symbol interference. As a result, the transmission produces extremely low jitter. This property enables high bandwidth communications. Because the signal in the present transmission line does not take a full swing on the entire wire and no buffer is inserted, the power consumption is much less than the RC wires with repeaters. In addition, the present transmission line can be implemented by using simple sender and receiver circuits to simplify the over structure and the fabrication. As a further example of the advantages, there are no active components between the sender and the receiver in the present transmission line so that the system tends to be robust against process, voltage and temperature variations.

[0039] Referring back to FIG. 2A, the leakage resistors 201 may be implemented in various configurations. In one example, a leakage resistor 201 can be a poly resistor as shown in the insert (a) in FIG. 6. Various structures and fabrication processes for poly resistors and unsilicided poly resistors are known. In another example shown in the insert (b) in FIG. 6, a leakage resistor 201 may also be a diffusion resistor formed from two connected transistors. In some implementations, the unsilicided poly resistor may be preferred because it occupies less area and has a better voltage-current linearity than some diffusion resistors. The sheet resistance of an unsilicided poly resistor can be as high as 1000 ohm/square in some implementations.

[0040] Other high resistive materials can also be used to construct the leakage resistors. For example, various metal resistors may be used as the leakage resistors. For another example, TaN or WSi may also be used to construct the leakage resistors. See "Integration of Mixed-Signal Elements into a High-Performance Digital CMOS Process" by K. J. Kuhn, et al. in Intel Technology Journal, vol. 6, issue 02, pp.31-42 (2002), and "WSi Sub(X) Thin Film for Resistors" by C. J. Backhouse, et al. in THIN SOLID FILMS. Vol. 311, no. 1-2, pp. 299-303 (1997). Consider using a typical 3μm wide copper wire at metal 6 for the differential transmission line based on the 90-nm technology. If a leakage resistor formed by a poly wire with a minimal width of e.g., 100 nm, is inserted in the differential transmission line every 200 μm, the leakage conductors for a 20-mm long link uses only 126 μm^2 of poly area.

[0041] For on-chip wires, the attenuation of the signal is exponentially proportional to the wire resistance. Hence, reducing the wire resistance is important to reducing the signal attenuation. A small attenuation can be used to simplify the receiver, to reduce the power consumption of the system, and improve the robustness against the crosstalk and other variations. One design to reduce the wire resistance is to use two or more pairs of differential wires to carry the same signal.

[0042] FIG. 7A shows one example where a first pair of conductor wires 711 and 722 and a second pair of conductor wires 721 and 722 are used to form a differential transmission line to carry the same signal. This design can be considered as splitting each wire in the two wires for a differential pair into two or more wires to increase the total cross section area of the transmission line. Because the wire resistance is inversely proportional to the cross section area, this splitting wire design can reduce the wire

resistance. Both wires 711 and 721 are used to receive the same signal from the first output terminal of the signal driver 110 and the wires 721 and 722 are used to receive the same signal from the second output terminal of the signal driver 110. In this particular example, the wires 711, 712, 721 and 722 are in positioned in sequence from left to right in the same plane parallel to and between two conductor layers 701 and 702 as the power ground layers for the chip.

[0043] When the differential transmission line is used to transmit signals at high frequencies, e.g., in the multi-Giga hertz frequency range, the signal current in each conductor may crowd near the edge of the wires due to the skin effect. One consequence of this skin effect is the reduced effective cross section area in the conductor wire that is used by the current. Hence, simply widening the wires based on the splitting wire design in FIG. 7A may not generate the resistance reduction proportional to the routing area usage. For high-speed communications, a different split wire design as shown in FIG. 7B may be used where each wire (D- or D+) is dimensioned to have a wide side and a short side and the two wires are coupled to each other via their wide sides to reduce the skin effect. The two wires can be placed between two power /ground (P/G) conductor layers which are parallel to the wide sides of the two wires. Another design for high-speed communications is shown in FIG. 7C where a single conductor strip line is placed between two power /ground conductor layers parallel to the wide side of the single conductor in the middle to reduce the skin effect and the wire resistance.

[0044] FIGS. 8A and 8b show two additional examples of differential transmission lines in split wire configurations. FIG. 8A uses two differential pairs between two power/ground conductors to form a differential transmission line but use a different spatial arrangement from the design in FIG. 7A. FIG. 8B is a variation from the design in FIG. 7B.

[0045] The differential transmission lines described here are waveguides and use at least two conductors to transmit signals. Various other configurations are possible. For example, a two-conductor waveguide often being referred as "a stripline" is a special form of the differential transmission line and can be used to incorporate the present leakage resistors to for distortionless transmission. In one implementation, such a stripline may include a conductor stripline and a power or ground shield to transmit an electrical signal. The leakage resistors may be connected between the conductor stripline and shield at different positions along the transmission line to make a phase velocity and a signal attenuation of the electrical signal to be independent of a frequency of the electrical signal.

[0046] To further illustrate the operation of the present distortionless differential transmission line, FIG. 9 shows the cross section view of an exemplary design along the direction perpendicular to the transmission line. The periodically located leakage resistors are not shown. In this design, a pair of edge-coupled stripe lines 910 and 920 made of copper are placed between low resistive upper and lower power /ground metal layers 901 and 902. Each of the wires 910 and 920 is 1 μm thick along the direction perpendicular to the layers 901 and 902 and has a width of 4 μm along the direction parallel to the layers 901 and 902. The separation between the wires 910 and 920 is also 4 μm. The wires 910 and 920 are separated from the power/ground plane layers by 1.5 μm.

[0047] In the design in FIG. 9, the unit length resistance, inductance, and capacitance values, *R, L, C,* of wires can be obtained by using a 3-D field solver. These values are, R = 4.4Ω/*mm*, L = 1.262 *nH/mm*, and C = 196.*418f F/mm*. The characteristic impedance of the differential pair is 84.5 x 2 = 169Ω. The number of leakage resistors (stages) inserted between the wires range from 4 to 200. For a pair of 2-cm

long wires, in order to match the *RLC* values to achieve distortionless transmission, the total leakage conductance is $6.15 \times 10^{-4} S$. The resistance of each leakage resistor ranges from $6.5k\Omega$ to $325k\Omega$. Assuming a 1.0V swing level at the sender side, the signal amplitude at the receivers side is 365 mV..

[0048] For each wire segments, the Agilent ADS Momentum is used to extract the 4-port S-parameter description. Then, a transient analysis of the circuit is performed using the HSpice software. A total of $2^{10} - 1 = 1023$ bits pseudo random bit sequences (PRBS) is generated as the input signal to the transmission line. The initial bit vector of PRBS is 1010101, and the generation polynomial is $x^7 + x + 1$. The clock frequency is set to 15 GHz, and each of the rising and falling transitions uses 10% of the clock cycle.

[0049] Simulations of the distortionless transmission lines with different number of leakage resistors are shown in TABLE I. The jitters of output voltages and the usage of the poly area are listed for different number of leakage resistors used in the transmission line. When the number of stages increases from 4 to 160, the jitter reduces from 27 ps to 2.08 ps. In the meanwhile, the poly area usage increases from 0.52 μm^2 to 832 μm^2.

[0050] FIGS. 10 and 11 show the eye diagrams of the output signals for distortionless transmission line with 4 stages and 120 stages of leakage resistors, respectively. When the there are only 4 resistors inserted into the distortionless line, the signal quality degrades as shown in FIG. 10. When the number of shunt resistors increases to 120, the transmission line achieves almost distortionless transportation, the data dependent jitter is only 2.1 ps (FIG. 11).

[0051] TABLE II further shows the effect of different configurations of wire geometries for the design in FIG. 9. The power consumption and signal attenuation are listed for transmission through a 2-cm long transmission line with

different wire widths and separations. The driver is designed to ensure the signal magnitude at the receiver end to be no less than 150 mV. The wires are terminated at the receivers end. When wider wires are used, the attenuation is reduced and so is the power consumption.

[0052] The above and other implementations of distortionless differential transmission lines may be used to interconnect various electronic elements, device, and modules. The data communication busses between CPUs, digital signal processors, memory banks, and others, are a few examples of the applications.

[0053] FIG. 12 shows one example of a clock distribution circuit on a chip using distortionless differential transmission lines. A clock signal source 1210 supplies the clock signal to be distributed to two or more locations on the chip. A distortionless differential transmission line 1220 is connected to the source 1210 to receive and deliver the clock signal to an interconnect junction 1230. At the junction 1230, The transmission line 1230 is split into or connected to two other distortionless transmission lines 1231 and 1232. As such, the clock signal is split into a first clock signal to the transmission line 1231 to the first destination and a second clock signal to the transmission line 1232 to the second destination. Certainly, various other applications for the distortionless transmission lines are possible.

[0054] Only a few implementations are disclosed. However, other variations and enhancements may be made.

Claims

What is claimed is:

1. A device, comprising:

a first conductor and a second conductor to form a differential transmission line to transmit an electrical signal; and

a plurality of leakage resistors connected between the first and second conductors at different positions along the differential transmission line to make a phase velocity and a signal attenuation of the electrical signal to be independent of a frequency of the electrical signal.

2. A device as in claim 1, wherein the leakage resistors are equal in resistance.

3. A device as in claim 2, wherein each leakage resistor has a conductance per one unit length of RC/L, where R, C and L are effective resistance, capacitance and inductance of the differential transmission line per one unit length, respectively.

4. A device as in claim 3, wherein the leakage resistors are equally spaced from one another along the differential transmission line.

5. A device as in claim 4, wherein a spacing between two adjacent leakage resistors is equal to or less than $ct_p/20$, wherein t_p is a clock period of the electrical signal and c is a speed of light in a dielectric material surrounding the transmission line.

6. A device as in claim 2, wherein the leakage resistors are equally spaced from one another along the differential transmission line.

7. A device as in claim 1, further comprising:

a substrate on which the first and second conductors and the leakage resistors are formed,

wherein the first conductor is a power /ground conductor on the substrate.

8. A device as in claim 7, further comprising a second power /ground conductor on the substrate, wherein the second conductor is a conductor line located between the power /ground conductor and the second power /ground conductor.

9. A device as in claim 1, further comprising third and fourth conductors between which the differential transmission line locates.

10. A device as in claim 9, further comprising a second differential transmission line in parallel to the differential transmission line and comprising fifth and sixth conductors in parallel to the first and second conductors,

wherein the fifth conductor is positioned on one side of the second conductor opposite to the first conductor and the sixth conductor is positioned on one side of the fifth conductor opposite the second conductor, and

wherein the first and fifth conductors are at a common electrical potential with respect to each other at each position along the first and second differential transmission lines and the second and six conductors are at a common electrical potential with respect to each other at each position along the first and second differential transmission lines.

11. A device as in claim 10, further comprising:

a differential signal driver comprising first and second output terminals to generate the electrical signal, wherein the first output terminal is coupled to the first and fifth conductors and the second output terminal is coupled to the second and sixth conductors.

12. A device as in claim 1, wherein each leakage resistor is a poly resistor.

13. A device as in claim 1, wherein each leakage resistor is a diffusion resistor.

14. A device as in claim 1, further comprising:

a signal driver connected at one end of the differential transmission line to generate the electrical signal; and

a signal receiver connected to another end of the differential transmission line to receive the electrical signal.

15. A device as in claim 1, further comprising a microprocessor connected to one end of the differential transmission line.

16. A device as in claim 1, further comprising a memory circuit connected to one end of the differential transmission line.

17. A device as in claim 1, further comprising a clock signal generator connected to one end of the differential transmission line.

18. A device as in claim 1, further comprising a digital signal processing circuit connected to one end of the differential transmission line.

19. A device as in claim 1, wherein each leakage resistor is a resistive metal resistor.

20. A device, comprising:

a first conductor and a second conductor to form a differential transmission line to transmit an electrical signal; and

a plurality of leakage resistors connected between the first and second conductors at different positions along the differential transmission line, wherein each leakage resistor has a conductance per one unit length of RC/L, where R, C and L are effective resistance, capacitance and inductance of the differential transmission line per one unit length, respectively.

21. A device as in claim 20, wherein a spacing between two adjacent leakage resistors is equal to or less than $ct_p/20$, wherein t_p is a clock period of the electrical signal and c is a speed of light in a dielectric material surrounding the transmission line.

22. A method, comprising:

using at least two conductors to form a differential transmission line to guide a signal; and

connecting a plurality of leakage resistors at different locations along the differential transmission line to connect the two conductors to make the phase velocity and attenuation of the signal in the transmission line independent of a frequency of the signal.

23. The method as in claim 22, further comprising making each leakage resistor to have a conductance per one unit length of RC/L, where R, C and L are effective resistance,

capacitance and inductance of the differential transmission line per one unit length, respectively.

24. The method as in claim 22, further comprising making the leakage resistors evenly spaced along the differential transmission line.

FIG. 1A

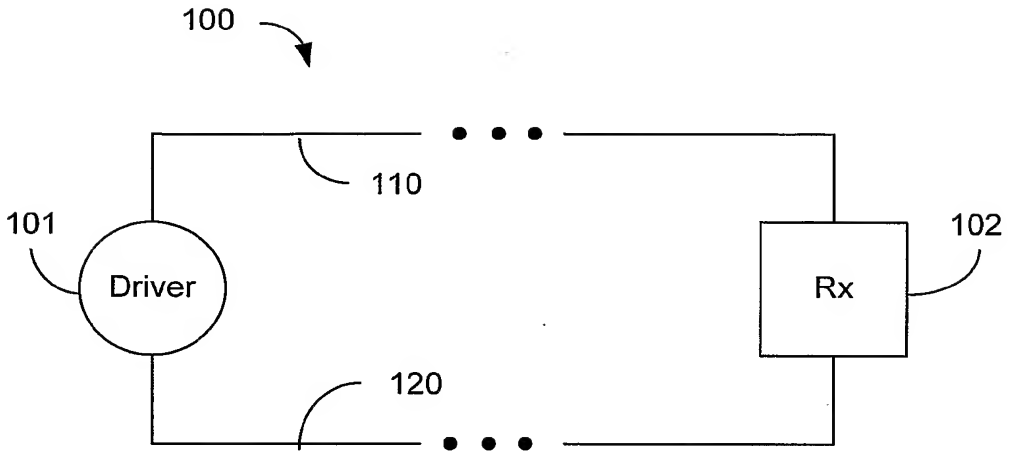

100
110
101
Driver
Rx
102
120

FIG. 1B

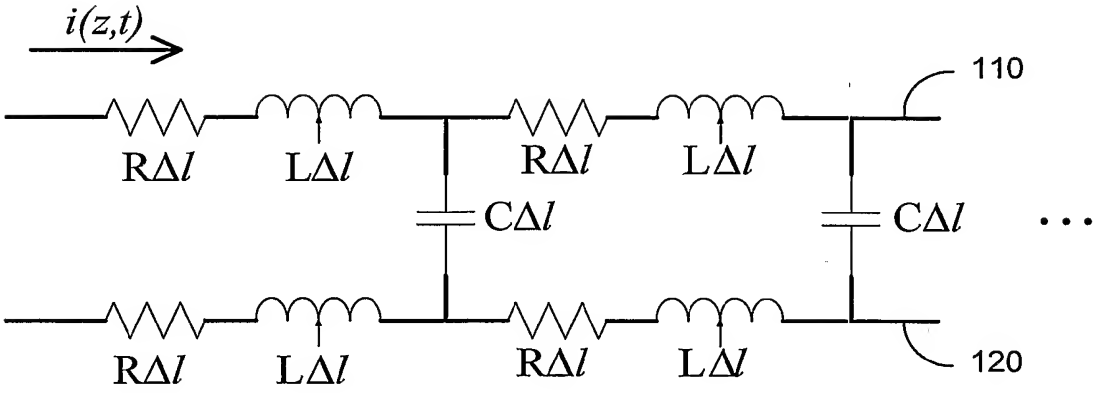

i(z,t)
110
RΔl
LΔl
RΔl
LΔl
CΔl
CΔl
RΔl
LΔl
RΔl
LΔl
120

FIG. 2A

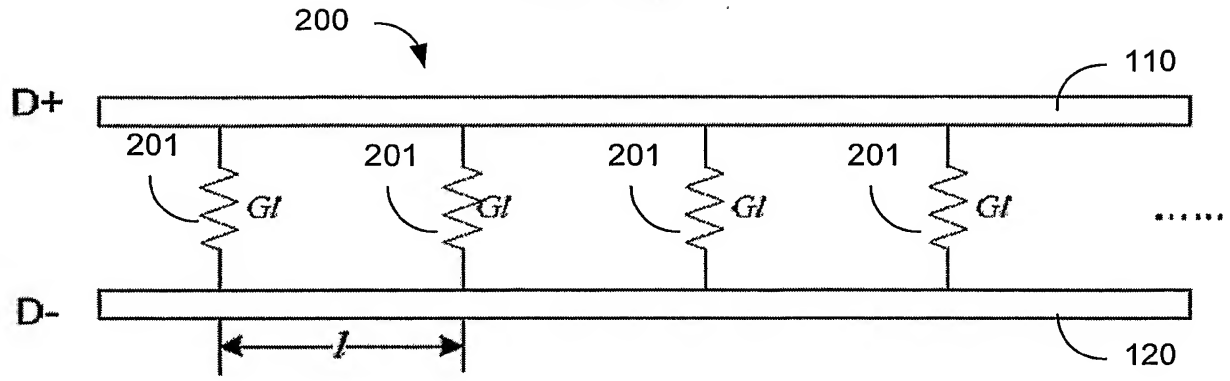


FIG. 2B

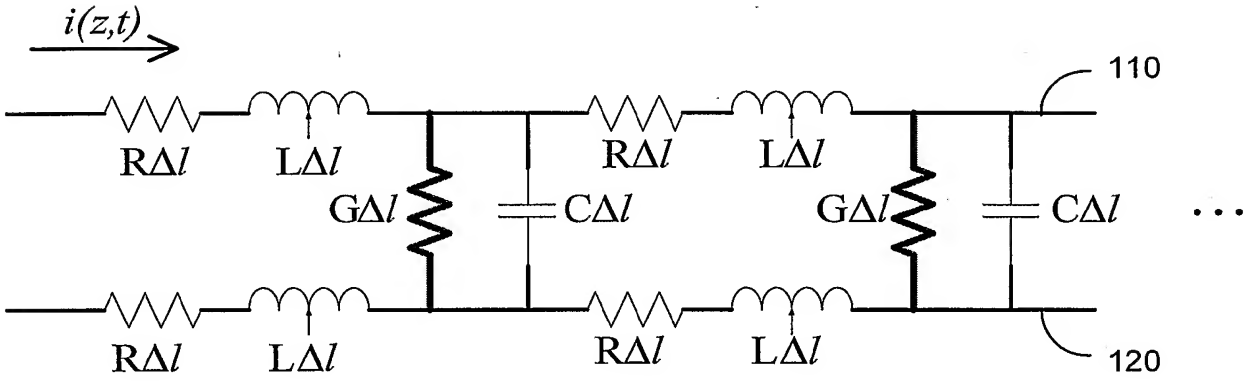


FIG. 2C

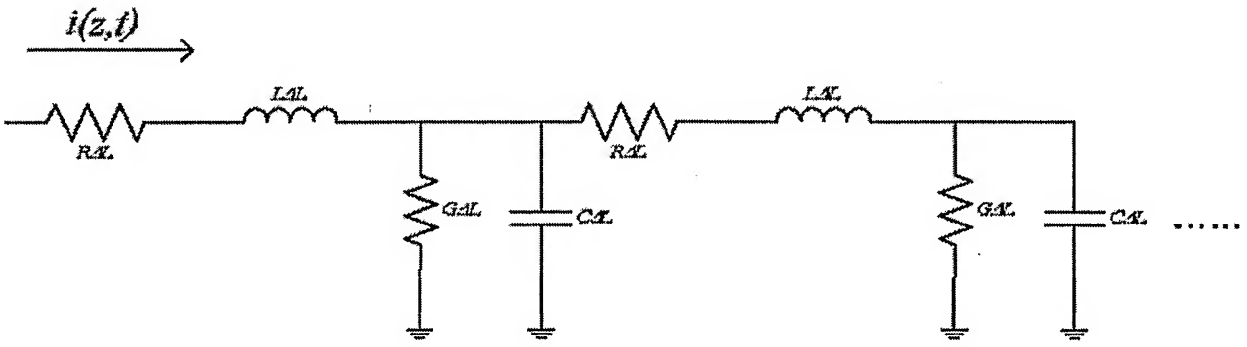


FIG. 3

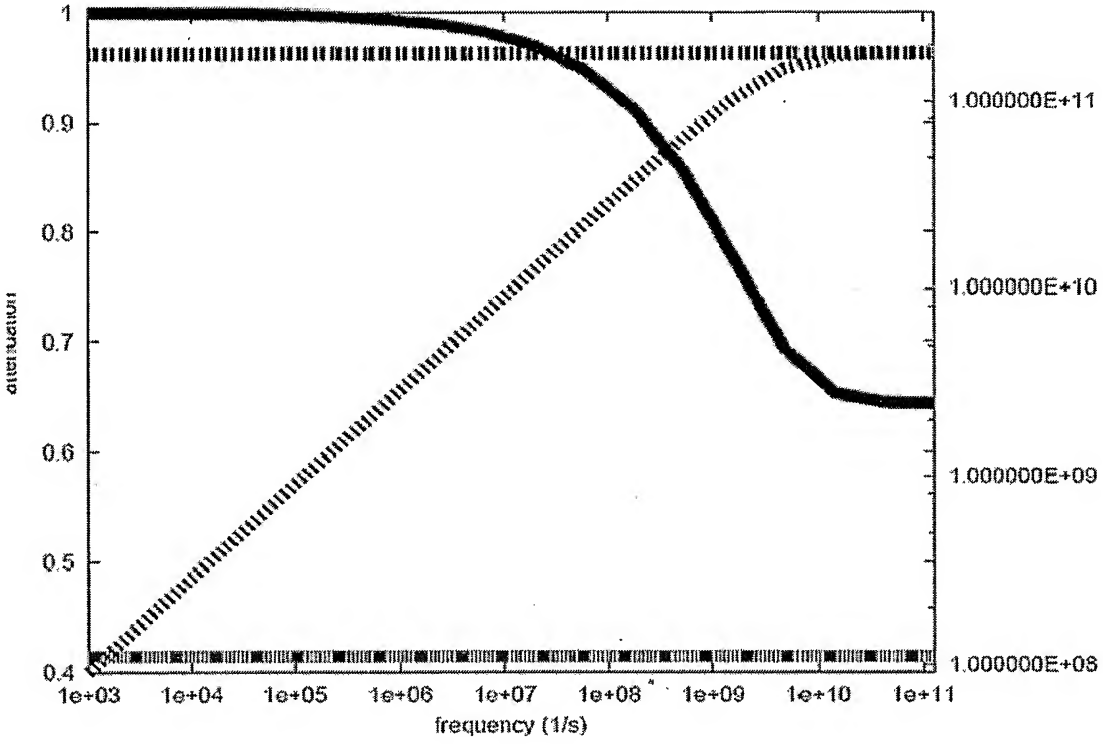

1
0.9
0.8
0.7
0.6
0.5
0.4
1.000000E+11
1.000000E+10
1.000000E+09
1.000000E+08
1e+03
1e+04
1e+05
1e+06
1e+07
1e+08
1e+09
1e+10
1e+11
frequency (1/s)

FIG. 4

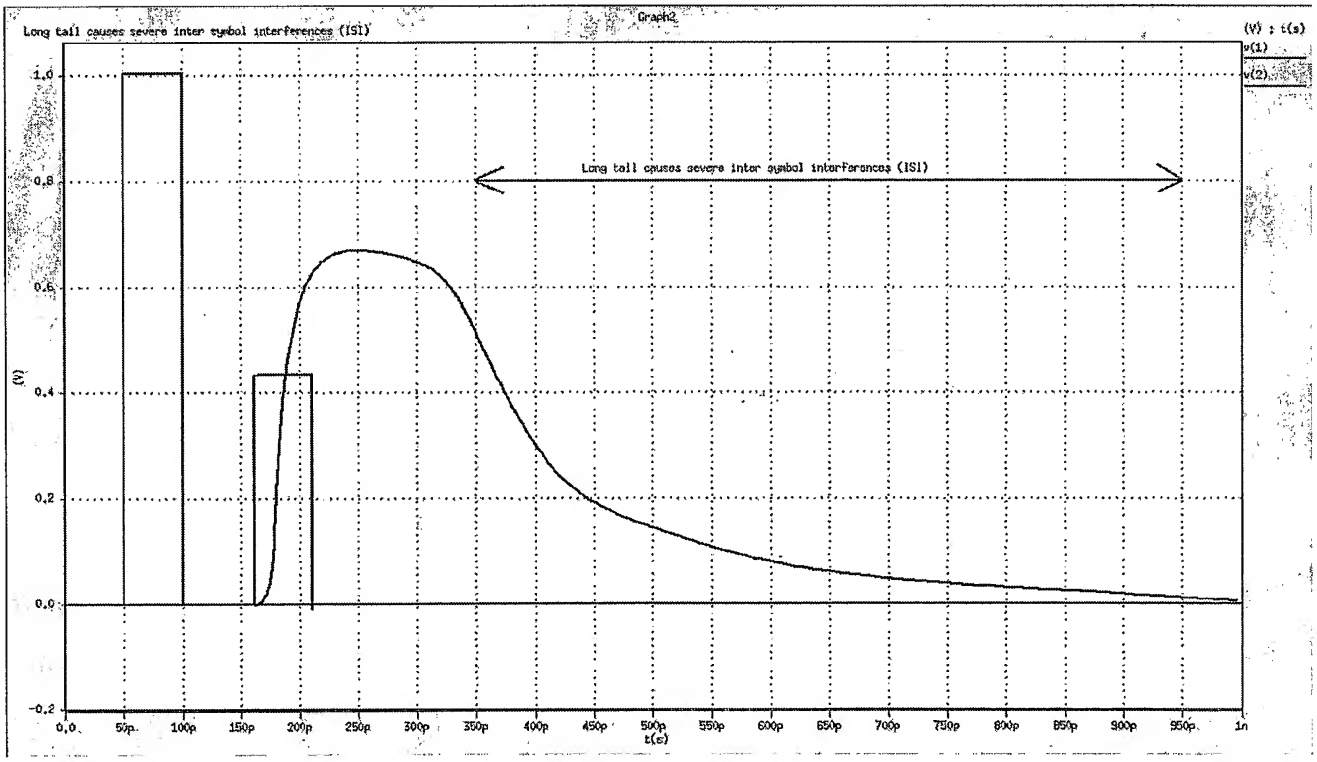

Long tail causes severe inter symbol interference (ISI)
Graph2
Long tail causes severe inter symbol interference (ISI)
(V)
t(s)

FIG. 5

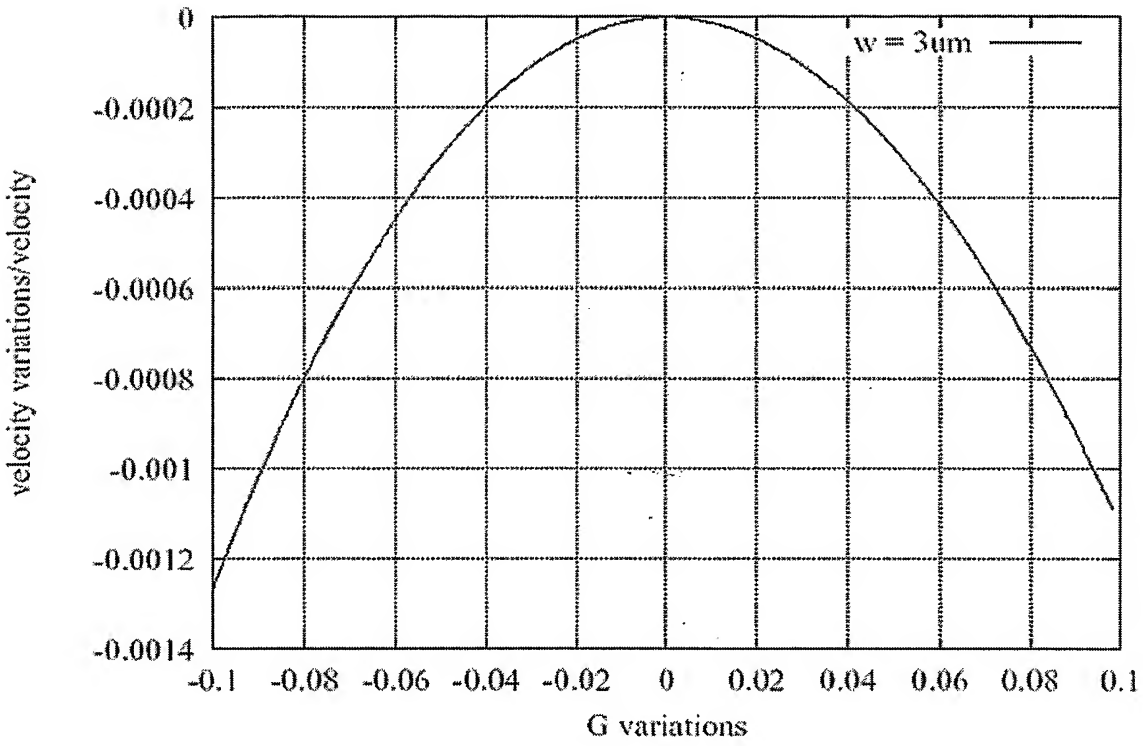

0
-0.0002
-0.0004
-0.0006
-0.0008
-0.001
-0.0012
-0.0014
velocity variations/velocity
w = 3um
-0.1
-0.08
-0.06
-0.04
-0.02
0
0.02
0.04
0.06
0.08
0.1
G variations

FIG. 6

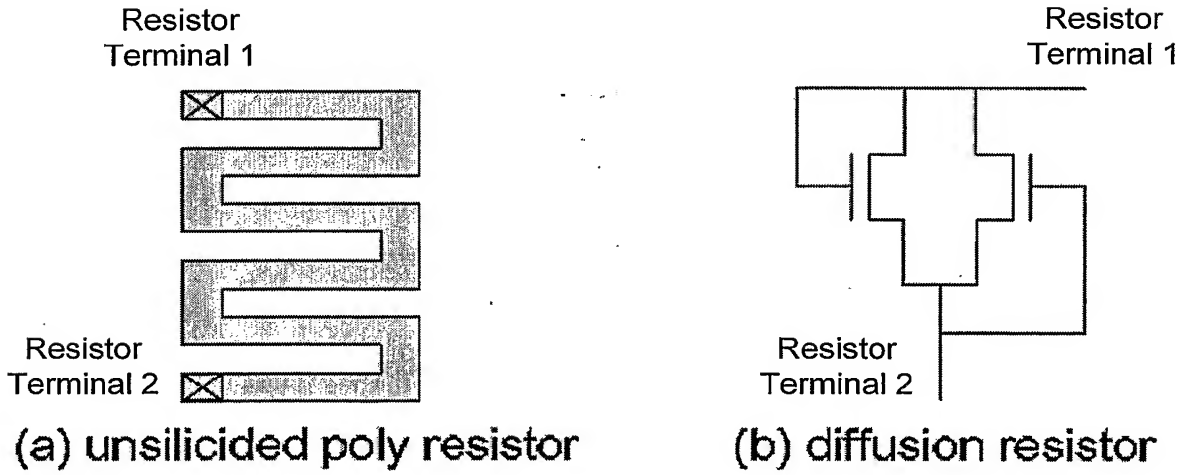

Resistor Terminal 1
Resistor Terminal 2
(a) unsilicided poly resistor
Resistor Terminal 1
Resistor Terminal 2
(b) diffusion resistor

FIG. 7A

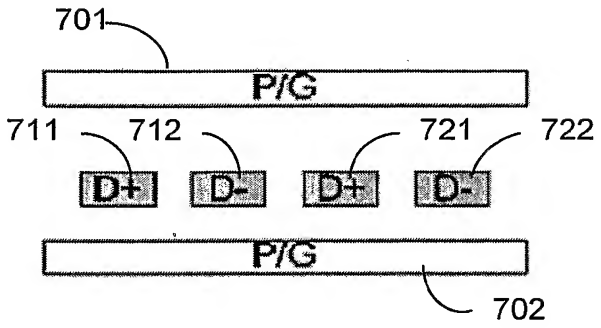


FIG. 7B

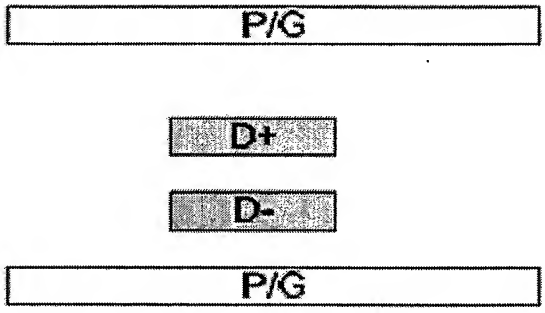


FIG. 7C

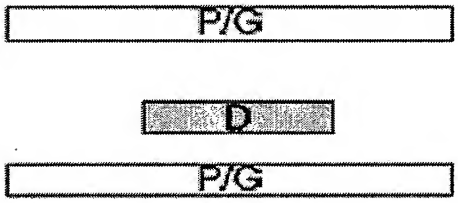


FIG. 8A

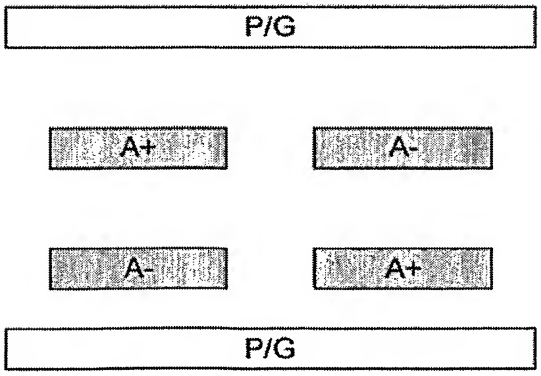


FIG. 8B

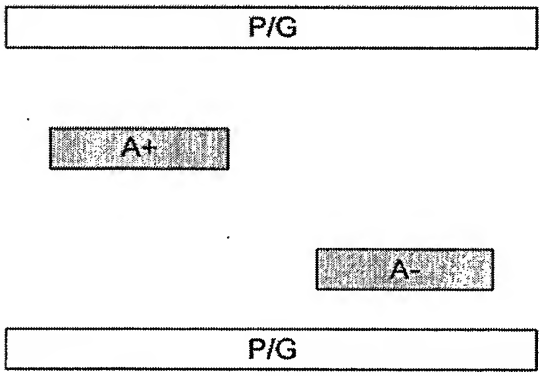


FIG. 9

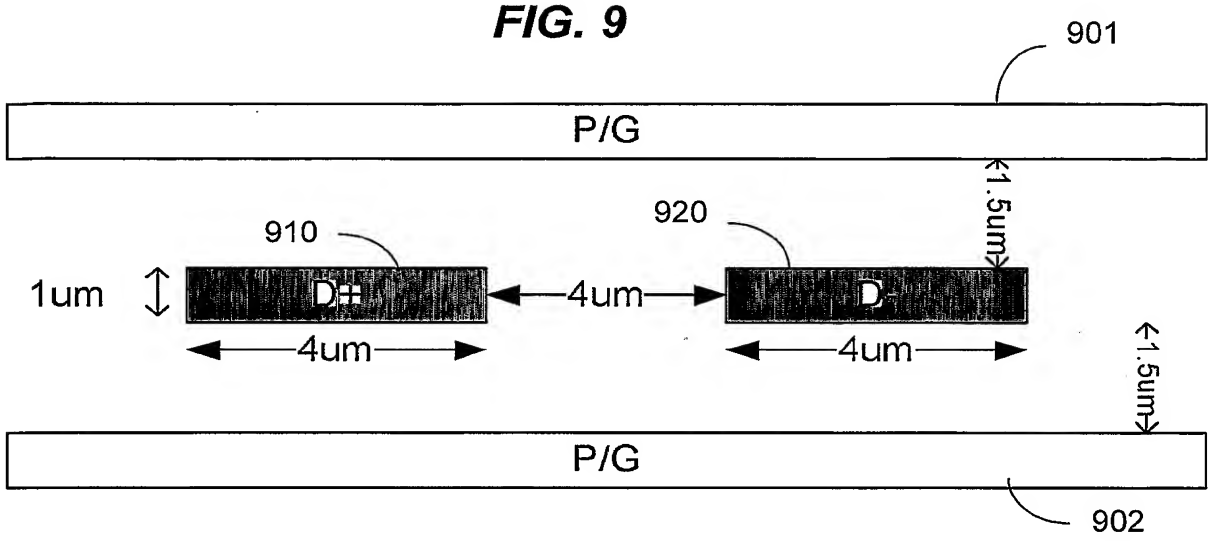


FIG. 10

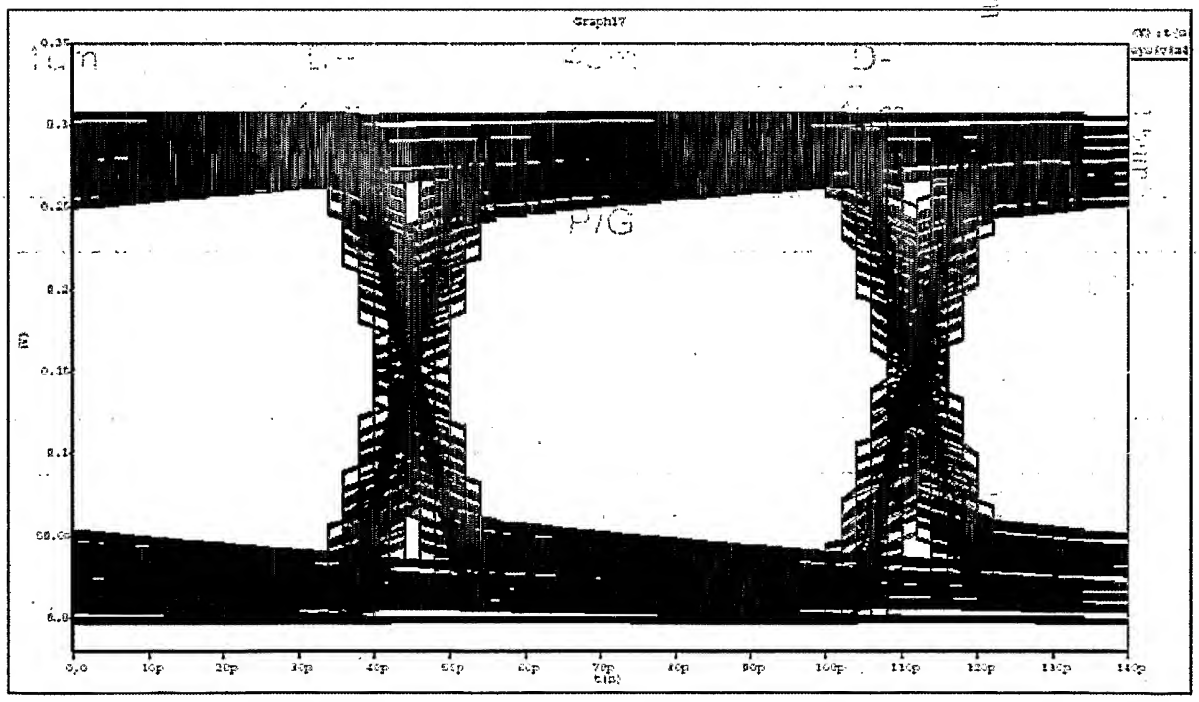


FIG. 11

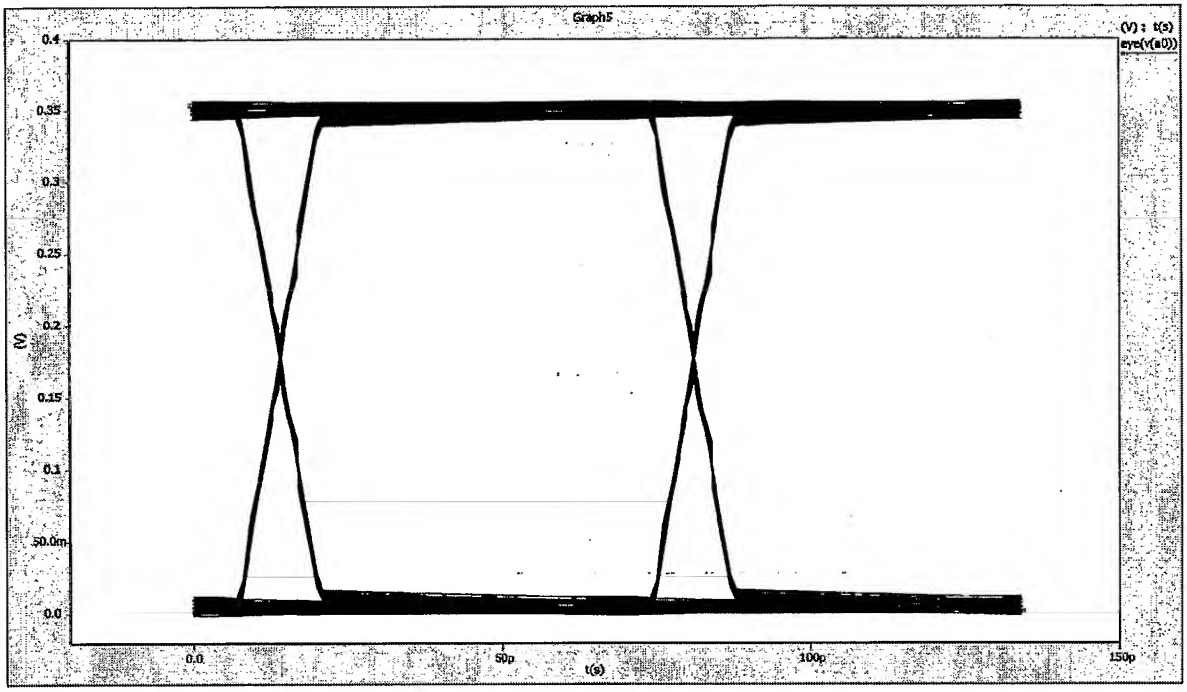
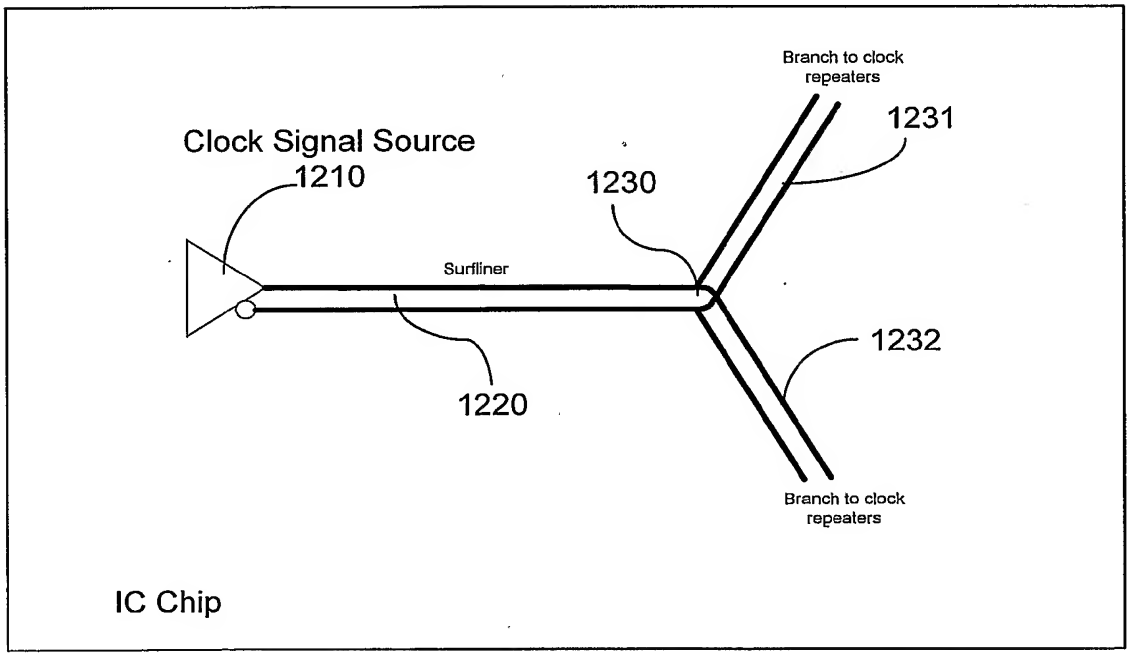

Graph5
(V) : t(s)
eye(v(a0))
0.4
0.35
0.3
0.25
0.2
0.15
0.1
50.0m
0.0
(V)
0.0
50p
t(s)
100p
150p

FIG. 12


Branch to clock repeaters
1231
Clock Signal Source
1210
1230
Surfliner
1232
1220
Branch to clock repeaters
IC Chip

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US05/23131

A. CLASSIFICATION OF SUBJECT MATTER
IPC: **G02B 6/42**(2006.01)

USPC: 398/202
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 398/202

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/0131135 A1 (CHOW et al.) 19 September 2002 (19.09.2002), entire document	1-24

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search
02 September 2006 (02.09.2006)

Date of mailing of the international search report
26 SEP 2006

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